IN THE CLAIMS

1-15. (Canceled)

16. (Currently Amended) A method for ~~polishing the surface of~~manufacturing a semiconductor device ~~substrate,~~ comprising the steps of:

forming a ~~transistor~~first conductive layer on ~~the~~a surface of a semiconductor substrate;

forming an insulating film so as to cover said ~~transistor~~first conductive layer and said surface of the semiconductor substrate;

holding the back surface of said semiconductor substrate with a substrate-holding carrier installed on a polishing equipment;

polishing said ~~substrate~~insulating film so that the reaction force, to said semiconductor substrate, generated when said semiconductor substrate is pushed against an inner guide provided so as to surround said semiconductor substrate for preventing said semiconductor substrate from deviating from said carrier due to a friction force generated by the relative movement between said semiconductor substrate and a polishing member provided on said polishing equipment, is dispersed, when said semiconductor substrate is rotated while being integrated with said carrier while holding said semiconductor substrate, and pushing said semiconductor

substrate against said polishing member provided in said polishing equipment, wherein an outer guide, which is separated from said inner guide at a position where said inner guide comes in contact with said semiconductor substrate, is provided outside of the inner guide in said carrier for keeping said carrier at a distance from said polishing member;

then forming an opening to said insulating film for electrically connecting said ~~transistor and capacitor to said insulating film~~first conductive layer; and

forming a ~~metal~~ second conductive layer to be ~~a~~ ~~wiring~~connected to said first conductive layer.

17. (Currently Amended) The method for ~~polishing~~manufacturing the ~~surface of a~~ semiconductor device ~~substrate~~ according to claim 16, wherein said inner guide has a recessed groove on ~~the~~an inner wall thereof, and a constant distance is maintained between said polishing member and said recessed groove.

18. (Currently Amended) A method for ~~polishing the surface of~~manufacturing a semiconductor device ~~substrate having a transistor,~~ comprising the steps of:

forming a ~~transistor~~first conductive layer on a semiconductor substrate;

forming an insulating film on said ~~transistor~~first conductive layer and said semiconductor substrate;

holding the back surface of said ~~semi-conductor~~semiconductor substrate with a substrate-holding carrier installed on a polishing equipment; and

polishing said ~~substrate~~insulating film in the state where the back surface of said semiconductor substrate is held, using a polishing member that has a different diameter and a different center location from the diameter and center of rotation of said semiconductor substrate~~,~~ while preventing said semiconductor substrate from moving laterally with an inner guide provided around said semiconductor substrate and having an elastic body on ~~the~~an inner wall thereof, wherein an outer guide, which is spaced apart from said inner guide at a portion where said inner guide comes in contact with said semiconductor substrate, is provided outside of the inner guide in said carrier for keeping said carrier at a distance from said polishing member.

19. (Currently Amended) A method for ~~polishing the surface of~~manufacturing a semiconductor device ~~substrate having a transistor,~~ comprising the steps of:

forming a ~~transistor~~first conductive layer on a semiconductor substrate;

forming an insulating film on said ~~transistor~~first conductive layer and said semiconductor substrate;

forming an opening in said insulating film;

forming a ~~metal~~second conductive layer on said ~~semiconductor substrate~~first insulating film having said opening; and

holding a back surface of the semiconductor substrate by means of a carrier for holding the semiconductor substrate provided at a polishing equipment,

polishing said ~~metal~~second conductive layer so that the reaction force, to said semiconductor substrate, generated when said semiconductor substrate is pushed against an inner guide provided so as to surround said semiconductor substrate for preventing said semiconductor substrate from deviating from said carrier due to a friction force generated by the relative movement between said semiconductor substrate and a polishing member provided on said polishing equipment, is dispersed, when said semiconductor substrate is rotated while being integrated with said carrier while holding said semiconductor substrate, and pushing said semiconductor substrate against said polishing member so as to leave the ~~metal~~second conductive layer in said opening, wherein an outer guide, which is spaced apart from said inner guide at a portion where said inner guide comes in contact with said semiconductor substrate, is provided outside of the inner

guide in said carrier for keeping said carrier at a distance from said polishing member.

20. (Currently Amended) A method for ~~polishing the surface of~~manufacturing a semiconductor device ~~substrate,~~ comprising the steps of:

forming a ~~transistor~~first conductive layer on a semiconductor substrate;

forming a first insulating film that has an opening for a contact hole, and a second insulating film that has a groove for wiring on said ~~transistor~~first conductive layer;

forming a ~~metal~~second conductive layer on said ~~semiconductor substrate that has said first and~~ second insulating film~~s~~ having said groove;

holding ~~the~~a back surface of said semiconductor substrate by means of a carrier for holding the semiconductor substrate provided at a polishing equipment; and

polishing said ~~metal~~second conductive layer in the state where the back surface of said semiconductor substrate is held, using a polishing member that has a different diameter and a different center of rotation from the diameter and center location of said semiconductor substrate, while preventing said semiconductor substrate from moving laterally with an inner guide provided around said semiconductor substrate and having an elastic body on ~~the~~an inner wall

thereof, so as to leave said ~~metal~~second conductive layer in said contact hole and groove, wherein an outer guide, which is spaced apart from said inner guide at a portion where said inner guide comes in contact with said semiconductor substrate, is provided outside of the inner guide in said carrier for keeping said carrier at a distance from said polishing member.

21. (Currently Amended) A method for ~~polishing the surface of~~manufacturing a semiconductor device ~~substrate having a transistor,~~ comprising the steps of:

forming a ~~transistor~~first conductive layer on ~~the surface of~~ a semiconductor substrate;

forming an insulating film so as to cover said ~~transistor~~first conductive layer;

holding a back surface of said semiconductor substrate by means of a carrier for holding the semiconductor substrate provided at a polishing equipment;

pushing the back surface of said semiconductor substrate against ~~the~~a surface of ~~the~~a polishing member by applying pressure to the back surface of said semiconductor substrate;

polishing said insulating film using said polishing member, while preventing a lateral movement of said semiconductor substrate caused by polishing processing

friction force generated between the semiconductor substrate and the polishing member with an inner guide placed around said semiconductor substrate and having a recess at a location that contacts with said semiconductor substrate, wherein an outer guide, which is spaced apart from said inner guide at a portion where said inner guide comes in contact with said semiconductor substrate, is provided outside of the inner guide in said carrier for keeping said carrier at a distance from said polishing member;

thereafter forming an opening for electrically connecting said ~~transistor and capacitor~~first conductive layer; and

forming a ~~metal~~second conductive layer ~~to be a wiring~~connecting said first conductive layer through said opening.

22-25. (Canceled).